REMARKS

Claims 1-33 were previously pending in this patent application. Claims 1-33 stand rejected. Herein, Claims 1, 3, 5, 7, 13-15, 18, 20, 26, and 28 have been amended. Accordingly, after this Amendment and Response, Claims 1-33 remain pending in this patent application. Further examination and reconsideration in view of the claims, remarks, and arguments set forth below is respectfully requested.

35 U.S.C. Section 102(e) Rejections

Claims 1-7 and 10-14 stand rejected under 35 U.S.C. 102(e) as being anticipated by Chen et al., U.S. Patent No. 6,757,882 (hereafter Chen). These rejections are respectfully traversed.

Independent Claim 1 recites, as amended:

> A computer implemented method of matching a selectable user module with plurality of programmable hardware resources associated with a predesigned programmable integrated circuit comprising:
> a. displaying said selectable user module, wherein ***said user module is a representation of a configuration of a programmable circuit for implementation on said predesigned programmable integrated circuit***;
> b. in response to a selection of said selectable user module, ***comparing a description*** of a hardware resource requirement of said programmable circuit of said selectable user module ***with a description*** of said plurality of programmable hardware resources associated with ***said predesigned programmable integrated circuit***; and
> c. using a result of said comparing ***to identify*** and ***to display*** a ***first allowed programmable hardware resource*** of the ***predesigned programmable integrated circuit satisfying*** the hardware resource requirement of said programmable circuit of said selectable user module. (emphasis added)

It is respectfully asserted that Chen does not disclose the present invention as recited in Independent Claim 1. In particular, Independent Claim 1

recites the limitations, "wherein ***said user module is a representation of a configuration of a programmable circuit for implementation on said predesigned programmable integrated circuit***," (emphasis added), "***comparing a description*** of a hardware resource requirement of said programmable circuit of said selectable user module ***with a description*** of said plurality of programmable resources associated with ***said predesigned programmable integrated circuit***," (emphasis added), and "using a result of said comparing ***to identify*** and ***to display*** a ***first allowed programmable hardware resource*** of the ***predesigned programmable integrated circuit satisfying*** the hardware resource requirement of said programmable circuit of said selectable user module," (emphasis added). Rather than being directed to implementing a design using a predesigned programmable integrated circuit and its programmable hardware resources as in Independent Claim 1, Chen is directed to facilitating a designer in designing and/or verifying SOC (system on a chip) using IP provided by a multitude of vendors. [Chen; Col. 3, lines 27-31].

More specifically, Chen is directed to efficiently selecting and employing the IP of IP packages (206) to form SOC designs and/or verify SOC designs. [Chen; Col. 4, lines 1-4]. The IP package (206) includes package description (210) and its constituting parts (220), wherein the package description (210) includes basic description (212) providing basic information about the IP of the IP package (206) and includes pins and bus related descriptions (214) providing physical and logical pin descriptions as well as bus implementation and decoding information to discern bus compatibility and connectivity for the IP of the IP package (206). [Chen; Figure 2; Col. 4, lines 11-29].

Further, elements 1302, 1304, 1308, and 1310 of Figure 13 are cited against Independent Claim 1 even though Figure 13 is directed to making available a design and/or verification environment based on a given IP platform for use by designers in the design of SOC. [Chen; Figure 13; Col. 11, lines 15-20]. This design and/or verification environment facilitates design of a SOC through aggregation of re-useable IP in an iterative and/or layered manner, by a designer. [Chen; Col. 11, lines 21-35]. The re-use of existing intellectual property (IP) modules provides a designer with the ability to gain the functionality of the re-used IP without the need to design the functionality as part of the new design. Id. Chen (as well as Figure 13) fails to disclose user module that is a representation of a configuration of a programmable circuit for implementation on the predesigned programmable integrated circuit, as in the invention of Independent Claim 1.

Moreover, Chen (as well as Figure 13) fails to disclose comparing a description of a hardware resource requirement of the programmable circuit of the selectable user module with a description of the plurality of programmable resources associated with the predesigned programmable integrated circuit, as in the invention of Independent Claim 1. On page 4 of the Office Action, a citation is made to a description reader (252) that identifies and reads pins and bus related description (214) but is silent as to comparing a description of a hardware resource requirement of the programmable circuit of the selectable user module with a description of the plurality of programmable resources associated with the predesigned programmable integrated circuit. Although a passage of Chen is cited on page 4 of the Office Action as teaching the comparison of the descriptions as in Independent Claim 1, the passage neither mentions comparison nor mentions description (of a hardware resource

requirement of the programmable circuit or of the plurality of programmable resources associated with the predesigned programmable integrated circuit) in an explicit or implicit manner.

Furthermore, a bus compatibility analyzer (254) that determines the bus architectures supported is cited against Independent Claim 1 as disclosing using a result of the comparing to identify and to display a first allowed programmable hardware resource of the predesigned programmable integrated circuit satisfying the hardware resource requirement of the programmable circuit of the selectable user module. However, determination of bus architectures supported is clearly different from using a result of a comparison, is clearly different from identifying and displaying a first allowed programmable hardware resource of the predesigned programmable integrated circuit, and is clearly different from satisfying the hardware resource requirement of the programmable circuit of the selectable user module, as in the invention of Independent Claim 1.

Therefore, it is respectfully submitted that Independent Claim 1 is not anticipated by Chen and is in condition for allowance.

Dependent Claims 2-7 and 10-14 are dependent on allowable Independent Claim 1, which is allowable over Chen. Hence, it is respectfully submitted that Dependent Claims 2-7 and 10-14 are patentable over Chen for the reasons discussed above.

Claims 15, 18-24, and 26-32 stand rejected under 35 U.S.C. 102(e) as being anticipated by Cooke et al., U.S. Patent Application Publication No. US2002/0016706 (hereafter Cooke). These rejections are respectfully traversed.

Independent Claim 18 recites, as amended:

> A computer implemented method of determining hardware resources for an electronic design comprising:
> a) ***selecting*** an electronic design ***represented as a user module of predefined functionality implementable on a predesigned programmable electronic device***;
> b) ***accessing a data description*** of hardware resources required ***for implementing said user module on said predesigned programmable electronic device***;
> c) ***accessing data descriptions*** of a plurality of pre-existing programmable hardware resources ***of said predesigned programmable electronic device on which to implement said user module***; and
> d) ***comparing said data description*** of said user module ***with said data descriptions*** of said plurality of pre-existing programmable hardware resources ***to automatically determine potential placement options of said user module on said predesigned programmable electronic device***, wherein ***each potential placement option represents one or more of said pre-existing programmable hardware resources selected to implement said user module***. (emphasis added)

It is respectfully asserted that Cooke does not disclose the present invention as recited in Independent Claim 18. In particular, Independent Claim 18 recites the limitations, "***selecting*** an electronic design ***represented as a user module of predefined functionality implementable on a predesigned programmable electronic device***," (emphasis added), "***accessing a data description*** of hardware resources required ***for implementing said user module on said predesigned programmable electronic device***," (emphasis added), "***accessing data descriptions*** of a plurality of pre-existing programmable hardware resources ***of said predesigned programmable electronic device on which to implement said user module***," (emphasis added), and, "***comparing said data description...with said data***

descriptions...to automatically determine potential placement options of said user module on said predesigned programmable electronic device, wherein ***each potential placement option represents one or more of said pre-existing programmable hardware resources selected to implement said user module***," (emphasis added). Rather than being directed to implementing a design using a predesigned programmable electronic device and its pre-existing programmable hardware resources as in Independent Claim 18, Cooke is directed to designing an integrated circuit and creating and using an androgynous interface between electronic components of the integrated circuit. [Cooke; paragraph 0017].

Specifically, Cooke is directed to designing an integrated circuit (instead of using a predesigned programmable electronic device) by starting with hardware description languages to define functional components, proceeding with logic synthesis to convert the functional description into specific circuit implementation, and then proceeding to place and route to produce a physical layout file that is used as a design "blueprint" for fabrication of the integrated circuit. That is, functionality is implemented by defining it with hardware description languages at the start of the design

Continuing, a block and logic synthesis are cited as disclosing selecting an electronic design represented as a user module of predefined functionality implementable on a predesigned programmable electronic device, as in the invention of Independent Claim 18. However, logic synthesis is defined at page 9 of the Office Action as converting the functional description of the block into a specific circuit implementation of the block instead of being selecting an electronic design represented as a user module of predefined functionality

implementable on a predesigned programmable electronic device. Moreover, a foundation block at page 10 of the Office Action is identified as being a selectable user module of predefined functionality even though the foundation block is specified for the new integrated circuit instead of being predefined functionality implementable on a predesigned programmable electronic device.

Also, a layout database (195) and interfacing with the layout database (195) are cited as disclosing accessing a data description of hardware resources required for implementing the user module on the predesigned programmable electronic device, as in the invention of Independent Claim 18. However, Cooke is silent as to the predesigned programmable electronic device. Further, there is no discussion that the layout database (195) has data description of hardware resources required for implementing the user module, which is predefined functionality implementable on the predesigned programmable electronic device.

On page 9 of the Office Action, floorplan footprints are cited as disclosing accessing data descriptions of a plurality of pre-existing programmable hardware resources of the predesigned programmable electronic device on which to implement the user module, as in the invention of Independent Claim 18. Floorplan footprints are clearly different from data descriptions of a plurality of pre-existing programmable hardware resources of the predesigned programmable electronic device of Independent Claim 18.

Furthermore, Cooke fails to disclose comparing the data description of the user module with the data descriptions of the plurality of pre-existing programmable hardware resources of the predesigned programmable electronic device to automatically determine potential placement options of the user module

on the predesigned programmable electronic device, wherein each potential placement option represents one or more of the pre-existing programmable hardware resources selected to implement the user module, as in the invention of Independent Claim 18. On page 9 of the Office Action, a citation is made to paragraph 0036 as disclosing the above-mentioned claim limitation. However, this citation is silent as to comparing the data description of the user module with the data descriptions of the plurality of pre-existing programmable hardware resources of the predesigned programmable electronic device and is silent as to each potential placement option represents one or more of the pre-existing programmable hardware resources selected to implement the user module. Although a passage of Cooke is cited on page 10 of the Office Action as teaching the comparison of the descriptions as in Independent Claim 18 and the automatic determination of the potential placement options as in Independent Claim 18, the passage does not discuss comparison, data descriptions (of hardware resources required for implementing the user module on the predesigned programmable electronic device or of a plurality of pre-existing programmable hardware resources of the predesigned programmable electronic device on which to implement the user module), predesigned programmable electronic device, and potential placement options in an explicit or implicit manner.

Therefore, it is respectfully submitted that Independent Claim 18 is not anticipated by Cooke and is in condition for allowance.

Dependent Claims 19-24 are dependent on allowable Independent Claim 18, which is allowable over Cooke. Hence, it is respectfully submitted that

Dependent Claims 19-24 are patentable over Cooke for the reasons discussed above.

With respect to Independent Claims 15 and 26, it is respectfully submitted that Independent Claims 15 and 26 recite similar limitations as in Independent Claim 18. Therefore, it is respectfully submitted that Independent Claims 15 and 26 are not anticipated by Cooke and are in condition for allowance for reasons discussed above.

Dependent Claims 27-32 are dependent on allowable Independent Claim 26, which is allowable over Cooke. Hence, it is respectfully submitted that Dependent Claims 27-32 are patentable over Cooke for the reasons discussed above.

35 U.S.C. Section 103(a) Rejections

Claims 8 and 9 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al., U.S. Patent No. 6,757,882 (hereafter Chen) in view of PSoC Designer: Integrated Development Environment User Guide Revision 1.09 (hereafter Guide 1.09). These rejections are respectfully traversed.

Dependent Claims 8 and 9 are dependent on allowable Independent Claim 1, which is allowable over Chen. Moreover, Guide 1.09 fails to teach, motivate, or suggest the limitations not disclosed by Chen. Hence, it is respectfully submitted that Independent Claim 1 is patentable over the

combination of Chen and Guide 1.09 for the reasons discussed above. Since Dependent Claims 8 and 9 depend from Independent Claim 1, it is respectfully submitted that Dependent Claims 8 and 9 are patentable over the combination of Chen and Guide 1.09 for the reasons discussed above.

Claims 16, 17, 25, and 33 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Cooke et al., U.S. Patent Application Publication No. US2002/0016706 (hereafter Cooke). These rejections are respectfully traversed.

Dependent Claims 16 and 17, Dependent Claim 25, and Dependent Claim 33 are dependent on allowable Independent Claims 15, 18, and 26, respectively, which are allowable over Cooke. Hence, it is respectfully submitted that Dependent Claims 16 and 17, Dependent Claim 25, and Dependent Claim 33 are patentable over Cooke for the reasons discussed above.

CONCLUSION

It is respectfully submitted that the above claims, arguments and remarks overcome all rejections and objections. All remaining claims (Claims 1-33) are neither anticipated nor obvious in view of the cited references. For at least the above-presented reasons, it is respectfully submitted that all remaining claims (Claims 1-33) are in condition for allowance.

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,

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Dated: 11/1/2006

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